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Reg. No. : .....

Name : .....

Third Semester B.Tech. Degree Examination, January 2016
(2013 Scheme)
13.306 : DIGITAL ELECTRONICS (T)

Time : 3 Hours Max. Marks : 100

PART – A

Answer **all** questions. **Each** question carries **2** marks.

1. Find the compliment of $\left[(a\bar{b} + c)\bar{d} + e \right]$.
2. What is a full adder ?
3. Draw the internal architecture of IC 7492.
4. Differentiate between Max term and Min term.
5. Differentiate between Latches and Flip Flops.
6. Show how SR flip flop can be converted into JK flip flop.
7. Write down the characteristic equation of JK flip flop.
8. Explain the working of a static RAM cell.
9. What do you mean by noise margin of a logic family ?
10. Draw the circuit of a 2 input CMOS NAND gate. **(10×2 = 20 Marks)**

PART – B

Answer **any one** question from **each** Module. **Each full** question carries **20** marks.

Module – I

11. a) Implement the expression using a 8 : 1 MUX
f (a, b, c, d) = Σm (0, 2, 3, 6, 8, 9, 12, 14). **6**

b) Using Quine-McCluskey method simplify the logic expression
f (a, b, c, d) = Σm (1, 3, 5, 8, 9, 11, 15) + d (2, 13). **14**

P.T.O.

12. a) Prove the universal property of NAND gate. 8

b) Find the SOP and POS expression for

$f(s, b, c, d) = (\bar{a}+\bar{b}+c+d)(a+\bar{b}+c+d)(a+b+c+\bar{d})$
$(a+b+\bar{c}+\bar{d})(\bar{a}+b+c+\bar{d})(a+b+\bar{c}+d)$ 5

c) Write a note on BCD to seven segment decoder. 7

Module – II

13. a) Design a synchronous self starting counter to count the sequence 1, 3, 5, 7, 9, 11, 13, 15, 1, 3,..... using JK flip flops. 14

b) Design an astable multi vibrator for a frequency of 1.2 KHz using 555 IC. 6

14. a) Design a flip flop with inputs A_n and B_n using T flip flop. The truth table of $A_n - B_n$ is

A_n	B_n	Q_{n+1}
1	1	Q_n
0	0	$\bar{Q}_n$
0	1	1
1	0	0

12

b) Design a monostable multivibrator for a pulse width of 1 ms using 555 IC. 8

Module – III

15. a) Design a sequence detector to detect the sequence 1011 in a stream of bits. 15

b) Draw Moore and Mealy notation of a JK flip flop. 5

16. A sequential circuit has an input X and an output Z such that, the output is same as the input was two clock cycles before. For example.
X = 0 1 0 1 1 0 1 0 1 1 0 1 0 0 0 1
Z = 0 0 0 1 0 1 1 0 1 0 1 1 0 1 0 0
The first two values of Z are 0. Find a mealy state graph and table for the circuit. 20

Module – IV

17. a) Explain the interfacing of TTL and CMOS. 8

b) Write short notes on :

i) RAM

ii) ROM

iii) PROM

iv) EPROM. (4×3=12 Marks)

18. a) Explain the working of a dynamic RAM cell and give the advantages and disadvantages. 10

b) Write the VHDL codes for a half adder and a 4bit up counter. 10